A Cascaded Multilevel Inverter Based on Switched-Capacitor for High-Frequency AC Power Distribution System

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***Abstract*—The increase of transmission frequency reveals more merits than low- or medium-frequency distribution among different kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution system (PDS). However, it is complicated to obtain a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor-based cascaded multilevel inverter is proposed in this paper, which is constructed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched-capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly reduced by the increasing number of voltage levels. A symmetrical triangular waveform modulation is proposed with a simple analog implementation and low modulation frequency comparing with traditional multicarrier modulation. The circuit topology, symmetrical modulation, operation cycles, Fourier analysis, parameter determination, and topology enhancement are examined. An experimental prototype with a rated output frequency of 25 kHz is implemented to compare with simulation results. The experimental results agreed very well with the simulation that confirms the feasibility of proposed multilevel inverter.**

***Index Terms*—Cascaded H-Bridge, high-frequency ac (HFAC), multilevel inverter, switched capacitor (SC), symmetrical phase-shift modulation (PSM).**

I. Introduction

HIGH-FREQUENCY ac (HFAC) power distribution system (PDS) potentially becomes an alternative to traditional dc distribution due to the fewer components and lower cost. The existing applications can be found in computer [1], telecom [2], electric vehicle [3], and renewable energy microgrid [4], [5]. However, HFAC PDS has to confront the challenges from large power capacity, high electromagnetic interference (EMI), and severe power losses [6]. A traditional HFAC PDS is made up of a high-frequency (HF) inverter, an HF transmission track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommodate the requirement of point of load (POL). In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity is easy to be achieved by multilevel inverter with lower switch stress. Nonpolluted sinusoidal waveform with the lower total harmonic distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design [7]. HF power distribution is applicable for small-scale and internal closed electrical network in electric vehicle (EV) due to moderate size of distribution network and effective weight reduction [8]. The consideration of operation frequency has to make compromise between the ac inductance and resistance [9], so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application.

The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type [10], [11]. The former uses diodes to clamp the voltage level, and the latter uses additional capacitors to clamp the voltage. The higher number of voltage levels can then be obtained; however, the circuit becomes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges [12], [13]. The basic circuit is similar to the classical H-bridge DC–DC converter [14]. The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. However, the disadvantages confronted by cascaded structure are more switches and a number of inputs. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. Theoretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the applications of cost saving and input limitation.

A number of studies have been performed to increase the number of voltage levels. A switched-capacitor (SC) based multilevel circuit can effectively increase the number of voltage levels. However, the control strategy is complex, and EMI issue becomes worse due to the discontinuous input current [15]. A

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single-phase five-level pulsewidth-modulated (PWM) inverter is constituted by a full bridge of diodes, two capacitors and a switch. However, it only provides output with five voltage levels, and higher number of voltage levels is limited by circuit structure [16]. An SC-based cascaded inverter was presented with SC frontend and full bridge backend. However, both complicated control and increased components limit its application [17]. The further study was presented using series/parallel conversion of SC. However, it is inappropriate to the applications with HF output because of multicarrier PWM (MPWM) [18], [19]. If output frequency is around 20 kHz, the carrier frequency reaches a couple of megahertz. Namely, the carrier frequency in MPWM is dozens times of the output frequency. Since the carrier frequency determines the switching frequency, a high switching loss is inevitable for the sake of high-frequency output. A boost multilevel inverter based in partial charging of SC can increase the number of voltage levels theoretically. However, the control strategy is complicated to implement partial charging [20]. Therefore, it is a challenging task to present an SC-based multilevel inverter with high-frequency output, low-output harmonics, and high conversion efficiency [21].

Based on the study situation aforementioned, a novel multilevel inverter and simple modulation strategy are presented to serve as HF power source. The rest of this paper is organized as follows. The discussions of nine-level inverter are presented in Section II, including circuit topology, modulation strategy, operation cycle, and Fourier analysis. The parameter determination and loss analysis are discussed in Section III. The further enhancement of 13-level inverter is studied in Section IV. The performance evaluation accomplished by simulation and experiment is described in Section V followed by concluding remarks.

II. SC-Based Cascaded Inverter With Nine-Level Output

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are N_1 and N_2, respectively, the number of voltage levels is $2 \times N_1 \times N_2 + 1$ in the entire operation cycle.

A. Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter ($N_1 = 2$, $N_2 = 2$), where S_1, S_2, S_1', S_2' as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C_1 and C_2. $S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d}$ are the switching devices of cascaded H-Bridge. V_{dc1} and V_{dc2} are input voltage. D_1 and D_2 are diodes to restrict the current direction. $i_{\rm out}$ and v_o are the output current and the output voltage, respectively.

It is worth noting that the backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of the directions of output voltage and current. In other words, H-Bridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.

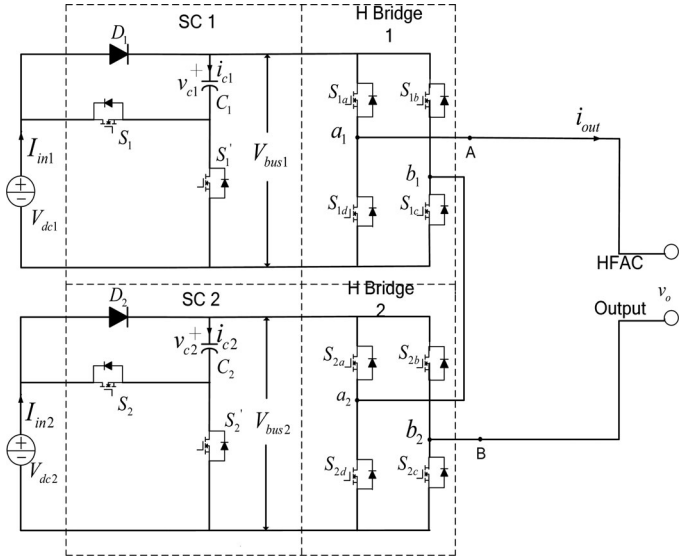


Fig. 1. Circuit topology of cascaded nine-level inverter ($N_1 = 2$, $N_2 = 2$).

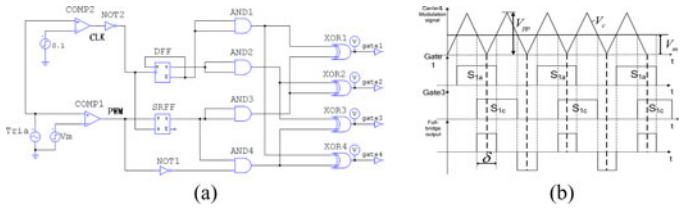


Fig. 2. Circuit and operational waveforms of symmetrical PSM. (a) Circuit of symmetrical PSM. (b) Operational waveforms of symmetrical PSM.

B. Symmetrical Modulation

There are many modulation methods to regulate the multilevel inverter, the popular modulations are the space vector modulation [22], the multicarrier PWM [23], and the selective harmonic elimination [24], [25], subharmonic pulsewidth modulation [26], etc. However, most of them greatly increase the carrier frequency that is dozens times the frequency of reference or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSM ensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency [27]. The structure of symmetrical PSM is shown in Fig. 2(a), and the operational waveform of symmetrical PSM is shown in Fig. 2(b).

The logic operations of gate signals are

$$\begin{aligned} \text{gate1} &= XOR\{Q(RS), \bar{Q}(D)\} \\ \text{gate2} &= XOR\{Q(RS), Q(D)\} \\ \text{gate3} &= XOR\{AND\{Q(RS), NOT(PWM)\}, Q(D)\} \\ \text{gate4} &= XOR\{AND\{Q(RS), NOT(PWM)\}, \bar{Q}(D)\}. \end{aligned} \tag{1}$$

(2)

A controlled PWM with pulsewidth δ is symmetrically generated by the comparisons of the triangle carrier V_c and modulation

signal V_m. The rising edge matching of V_c and V_m triggers the polarity inversion of the leading bridge, while the falling edge matching of V_c and V_m triggers the polarity inversion of the lagging bridge. When V_m has a change ΔV_m, this modulation simultaneously moves gate1 and gate3 in the opposite direction. Thus, the derived V_{ab} is symmetrical with respect to V_c.

C. Operation Cycles

Fig. 3 demonstrates the ideal waveforms of proposed inverter. V_c is the triangular carrier, and V_{pp} is the peak value of V_c. The modulation signals of triangular carrier are $V_{m\_1c}, V_{m\_1b}, V_{m\_2c}$ and V_{m_2b}. V_{m_1b} and V_{m_2b} are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and δ_i is the duration of voltage levels controlled by them. V_{m_1c} and V_{m_2c} are used to control the alternative operations of SC1 and SC2, respectively, and α_i is the duration of voltage levels controlled by them. Thus, the drive signals of H-Bridge switches $(S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d})$ are phase-shifted pulse signals, while the drive signals of SC switches (S_1, S_2, S_1', S_2') are complementary pulse signals. Two operational modes are presented as shown in Fig. 3(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals (V_{m_1c}, V_{m_1b}, V_{m_2c}, V_{m_2b}). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2.

Active circuits of the operational mode 1 are demonstrated in Fig. 4. R_e is the equivalent load. When t satisfies $t_0 \le t < t_1$ in Fig. 3(a), the switches $S_{1a}, S_{1b}, S_{2a}, S_{2b}$ are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because S_1' and S_2' are on, the capacitors C_1 and C_2 are charged to $V_{\rm in}$ $(V_{dc1} = V_{dc2} = V_{\rm in})$. The voltages on Bus 1 and Bus 2 are $V_{\rm in}$ as well. The current flow of this time interval is shown in Fig. 4(a).

When t satisfies $t_1 \le t < t_2$ in Fig. 3(a), the switches $S_{1a}, S_{1b}, S_{2a}, S_{2c}$ are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals $V_{\rm in}$. Because S_1' and S_2' are on, the capacitors C_1 and C_2 keep charged to $V_{\rm in}$ $(V_{dc1} = V_{dc2} = V_{\rm in})$. The voltages on Bus 1 and Bus 2 are $V_{\rm in}$ as well. The current flow of this time interval is shown in Fig. 4(b).

When t satisfies $t_2 \le t < t_3$ in Fig. 3(a), the switches $S_{1a}, S_{1c}, S_{2a}, S_{2c}$ are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $2V_{\rm in}$. Because S_1' and S_2' are on, the capacitors C_1 and C_2 keep charged to $V_{\rm in}$ $(V_{dc1} = V_{dc2} = V_{\rm in})$. The voltages on Bus 1 and Bus 2 are $V_{\rm in}$ as well. The current flow of this time interval is shown in Fig. 4(c).

When t satisfies $t_3 \le t < t_4$ in Fig. 3(a), the switches $S_{1a}, S_{1c}, S_{2a}, S_{2c}$ are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $3V_{\rm in}$. Because S_1' and S_2 are on, the capacitor C_1 keeps charged to $V_{\rm in}$ $(V_{dc1} = V_{dc2} = V_{\rm in})$, and the capacitor C_2 is discharged. The voltages on Bus 1 and Bus 2 are $V_{\rm in}$ and $2V_{\rm in}$, respectively. The current flow of this time interval is shown in Fig. 4(d).

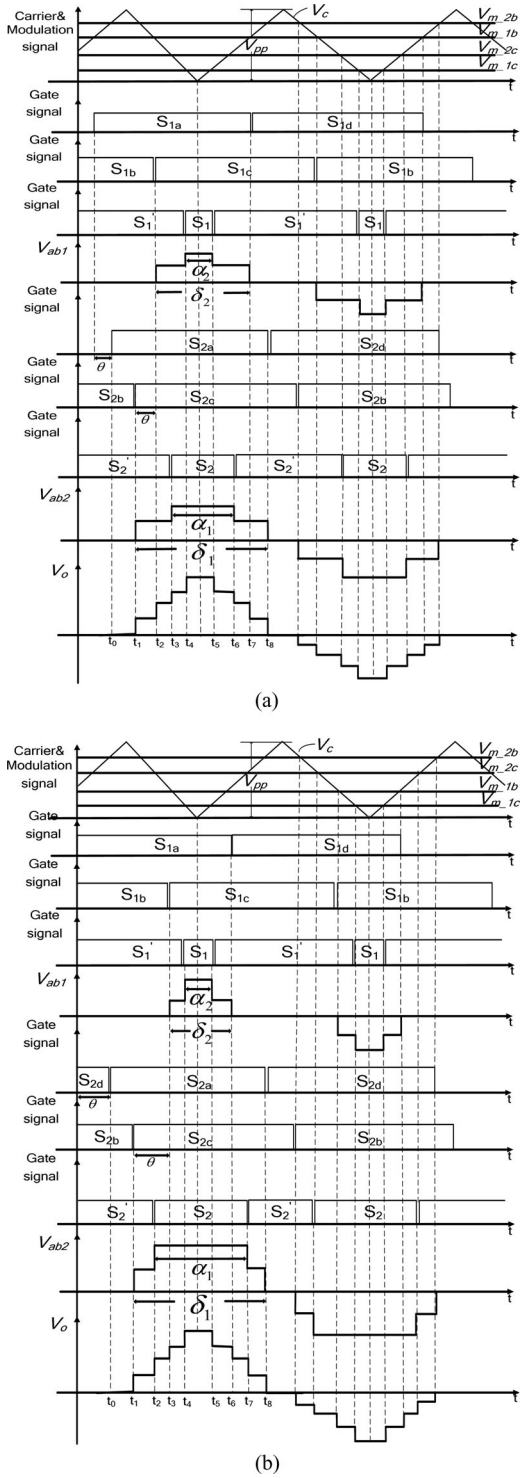


Fig. 3. Operational waveforms of the proposed multilevel inverter. (a) Operational mode 1. (b) Operational mode 2.

When t satisfies $t_4 \le t < t_5$ in Fig. 3(a), the switches $S_{1a}, S_{1c}, S_{2a}, S_{2c}$ are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $4V_{\rm in}$. Because S_1 and S_2 are on, the capacitor C_1 and C_2 are discharged. The voltages on Bus 1 and Bus 2 both are $2V_{\rm in}$. The current flow of this time interval is shown in Fig. 4(e).

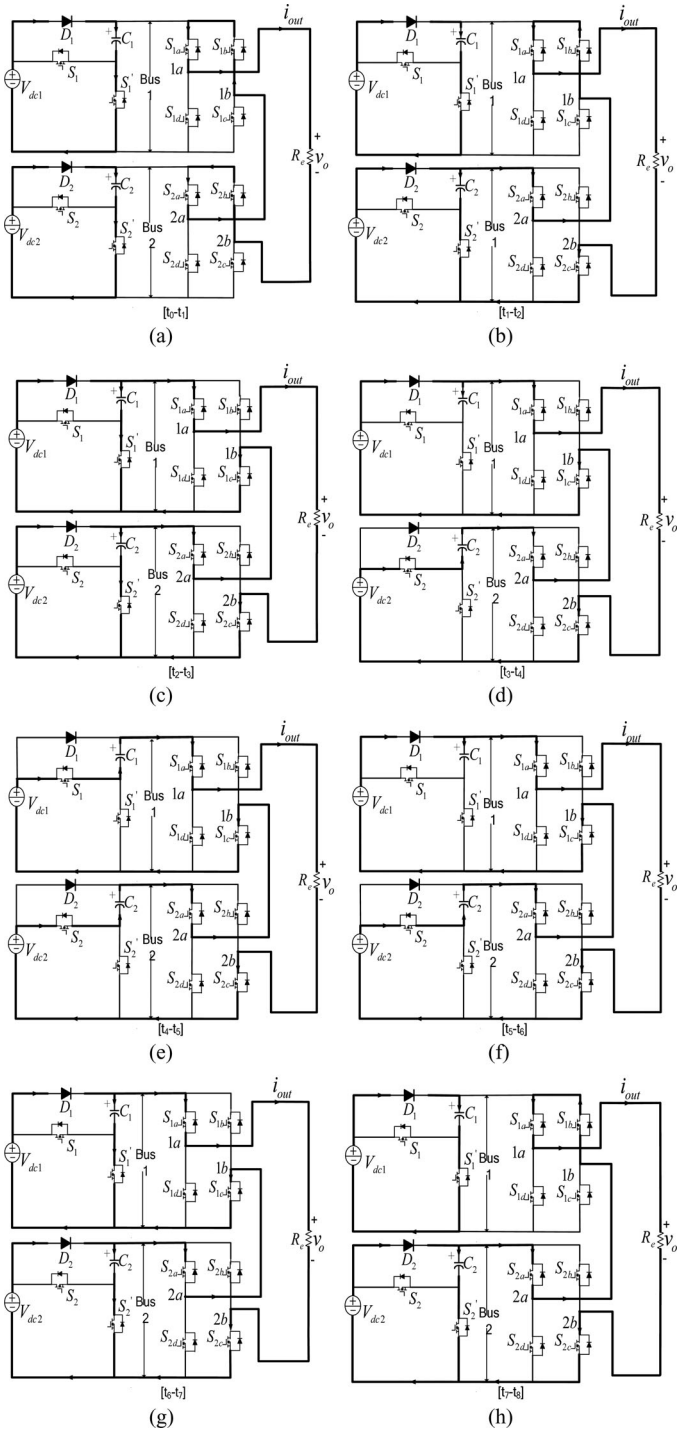


Fig. 4. Active circuits for different operation intervals in the operational mode 1: (a) $t_0 - t_1$; (b) $t_1 - t_2$; (c) $t_2 - t_3$; (d) $t_3 - t_4$; (e) $t_4 - t_5$; (f) $t_5 - t_6$; (g) $t_6 - t_7$; (h) $t_7 - t_8$.

The operations in $t_5 \leq t < t_6$, $t_6 \leq t < t_7$, and $t_7 \leq t < t_8$, are the same as the operations in $t_3 \leq t < t_4$, $t_2 \leq t < t_3$, and $t_1 \leq t < t_2$, respectively. The active circuits are shown in Fig. 4(f)–(h).

Comparing with operational mode 1, the mode 2 has the different active circuits in two time intervals. When t satisfies $t_2 \leq t < t_3$ in operational mode 2 as shown in Fig. 3(b), the switches $S_{1a}, S_{1b}, S_{2a}, S_{2c}$ are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals $2V_{\rm in}$. Because S_1' and S_2 are on, the capacitor C_1 keeps charged to $V_{\rm in}$ and capacitor C_2 is discharged. The voltages on Bus 1 and Bus 2 are $V_{\rm in}$ and $2V_{\rm in}$, respectively. The current flow of this time interval is shown in Fig. 5(a). Similarly, the active circuit of $t_6 \leq t < t_7$ is shown in Fig. 5(b) that has the same operations as $t_2 \leq t < t_3$.

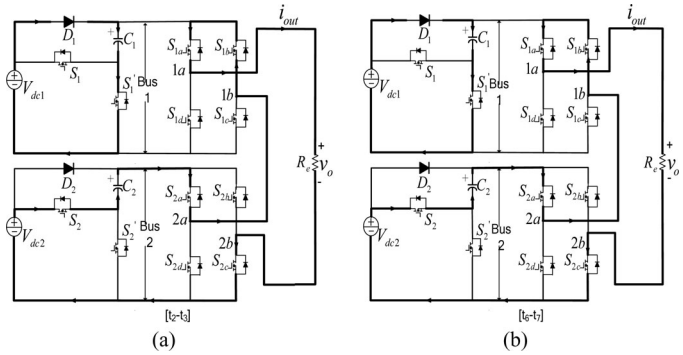


Fig. 5. Active circuits for different operation intervals in the operational mode 2: (a) $t_2 - t_3$; (b) $t_6 - t_7$.

The second half-cycle (from t_8 on) has the similar active circuits as the first half-cycle $(t_1 - t_8)$, but the current will be circulated in the opposite direction to provide the negative output voltage. The relations of on-state switches and output voltage level are described in Table I, as well as operations of two modes are compared closely. Table I has ten working states for nine voltage levels. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The device stress in switching devices of H-bridge circuit is higher than that in SC circuit. It can also be found that the output voltage in Mode 1 is more stable than Mode 2 due to less discharging period of switching capacitor.

Along with the up-down movement of modulation signals $(V_{m\_1c}, V_{m\_1b}, V_{m\_2c}, V_{m\_2b})$, the output voltage of the proposed inverter is a controllable nine-level staircase. The duration of each voltage level is determined by the duty-cycle of SC circuit and the phase-shifted angle of H-Bridge circuit.

D. Operation Cycles

In aforementioned nine-level inverter, the staircase output v_o can be divided into four components v_{01}, v_{02}, v_{03}, and v_{04}, as shown in Fig. 6. The durations of each component are decided by the comparisons of reference signal $(V_{m\_1c}, V_{m\_1b}, V_{m\_2c}, V_{m\_2b})$ and triangular carrier (V_c). If pulsewidths of the constituted component are defined as $\delta_1, \delta_2, \alpha_1$, and α_2, Fourier analysis is accomplished for this nine-level staircase.

The magnitude of the harmonics is derived by

$$V_n = \frac{4V_{\rm in}}{n\pi}\left(\cos\left(n\left(\frac{\pi-\alpha_1}{2}\right)\right) + \cos\left(n\left(\frac{\pi-\delta_1}{2}\right)\right) + \cos\left(n\left(\frac{\pi-\alpha_2}{2}\right)\right) + \cos\left(n\left(\frac{\pi-\delta_2}{2}\right)\right)\right), \quad n = 1,\ 3,\ 5,\ \ldots \tag{3}$$

TABLE I
RELATIONS OF ON-STATE SWITCHES AND OUTPUT VOLTAGE

Mode 1			Mode 2		
On-state switches	Output voltage	Capacitor State	On-state switches	Output voltage	Capacitor State
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1,S_2	$4V_{in}$	C_1, C_2 Discharging	S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1,S_2	$4V_{in}$	C_1, C_2 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2	$3V_{in}$	C_2 Discharging	S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1', S_2	$3V_{in}$	C_2 Discharging
S_{1a}, S_{1c}, S_{2a}, S_{2c}, S_1' S_2'	$2V_{in}$	C_1, C_2 Charging	S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2	$2V_{in}$	C_2 Discharging
S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'	V_{in}	C_1, C_2 Charging	S_{1a}, S_{1b}, S_{2a}, S_{2c}, S_1' S_2'	V_{in}	C_1, C_2 Charging
S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2' or S_{1c}, S_{1d}, S_{2c}, S_{2d}	0	C_1, C_2 Charging	S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_1' S_2' or S_{1c}, S_{1d}, S_{2c}, S_{2d}	0	C_1, C_2 Charging
S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'	$-V_{in}$	C_1, C_2 Charging	S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'	$-V_{in}$	C_1, C_2 Charging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2'	$-2V_{in}$	C_1, C_2 Charging	S_{1c}, S_{1d}, S_{2b}, S_{2d}, S_1' S_2	$-2V_{in}$	C_2 Discharging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2	$-3V_{in}$	C_2 Discharging	S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1', S_2	$-3V_{in}$	C_2 Discharging
S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1,S_2	$-4V_{in}$	C_1, C_2 Discharging	S_{1b}, S_{1d}, S_{2b}, S_{2d}, S_1,S_2	$-4V_{in}$	C_1, C_2 Discharging

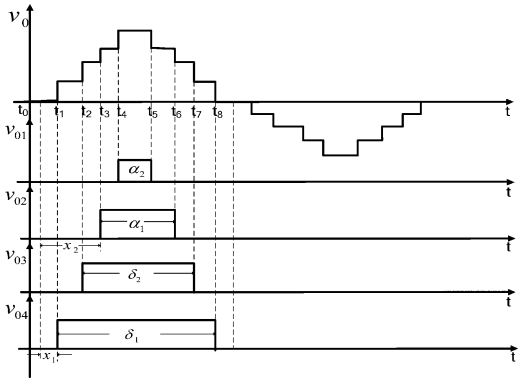


Fig. 6. Output voltage decomposition for Fourier analysis in mode 1.

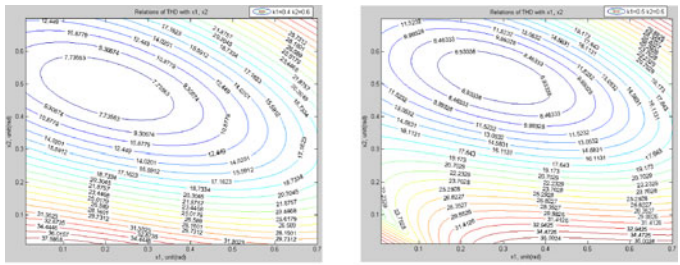


Fig. 7. Relation curves of output THD versus x_1, x_2 (unit, rad): (a) $k_1 = 0.6$, $k_2 = 0.4$; (b) $k_1 = 0.5$, $k_2 = 0.5$.

In operational mode 1

$$\delta_1 = \frac{V_{m\_2b}}{V_{pp}}\pi, \qquad \alpha_1 = \frac{V_{m\_1b}}{V_{pp}}\pi,$$
$$\delta_2 = \frac{V_{m\_2c}}{V_{pp}}\pi, \qquad \alpha_2 = \frac{V_{m\_1c}}{V_{pp}}\pi. \tag{4}$$

In operation mode 2

$$\delta_1 = \frac{V_{m\_2b}}{V_{pp}}\pi, \qquad \alpha_1 = \frac{V_{m\_2c}}{V_{pp}}\pi,$$
$$\delta_2 = \frac{V_{m\_1b}}{V_{pp}}\pi, \qquad \alpha_2 = \frac{V_{m\_1c}}{V_{pp}}\pi. \tag{5}$$

To further describe the relations of output THD and pulsewidths $\alpha_1, \alpha_2, \delta_1, \delta_2$, four parameters are predefined

$$k_1 = \frac{\alpha_1}{\delta_1}, \quad k_2 = \frac{\alpha_2}{\delta_2}, \quad x_1 = \frac{\pi - \delta_1}{2}, \quad x_2 = \frac{\pi - \delta_2}{2}. \tag{6}$$

The output waveforms can be characterized by these four constants. According to the definitions as $(\mathrm{THD} = (\sqrt{\sum_{n=2\ldots}^{\infty} V_n^2}/V_1) \times 100\%)$, THD of output voltage can be calculated by the harmonic magnitudes. The relations of output THD to x_1, x_2 are given in Fig. 7 with the fixed k_1 and k_2.

It can be found from Fig. 7 that THD is easy to be regulated by the duration width of voltage levels. At the suitable scope of x_1 and x_2, THD of output voltage is less than 10%. When $k_1 = 0.6$ and $k_2 = 0.4$, THD can be less than 10% within the scope of $0.05 < x_1 < 0.5$ and $0.4 < x_2 < 0.6$. When $k_1 = 0.5$ and $k_2 = 0.5$, THD can be less than 10% within the scope of $0 < x_1 < 0.4$ and $0.4 < x_2 < 0.6$. Furthermore, THD becomes less along with the increasing number of voltage levels. The output magnitude of multilevel inverter can be regulated by the duration width of voltage levels as well. Two patterns are available to perform the regulations of THD and magnitude simultaneously. One is to regulate x_1, x_2 with the fixed k_1, k_2. The other one is to regulate k_1, k_2 with the fixed x_1, x_2. The numerical benchmark and THD optimization will be examined in the future study, and a fixed ratio ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$) is adopted to evaluate output harmonics in subsequent simulation and experiment.

If the proposed dc–ac inverter is used as second stage of ac–ac conversion, an ac–dc controlled rectifier is introduced as preceding stage of ac–ac conversion. Power factor correction (PFC) implemented by dc–dc converter can improve the power factor in ac–dc conversion. In this case, both SC and H-bridge generate the optimized pulsewidth to minimize output THD. The magnitude regulation of output voltage can be performed by controllable ac–dc stage in input side. The minimized THD is achieved by this two-stage power circuit, namely, ac–dc stage is used to regulate magnitude, and dc–ac stage formed by the proposed inverter is used to minimize THD.

III. Determination of Capacitance

As shown in Fig. 4, the capacitors are charged when they are in parallel with power source, and the capacitors are discharged when they are in series with power source. The switch S_i and S_i' are driven alternatively during the half of output cycle. Therefore, the driven frequency of S_i and S_i' is twice the frequency of output voltage, as well as the driven frequency of $S_{ia} - S_{id}$ is the same as the frequency of output voltage.

The capacitance of C_i is determined by the voltage ripple of C_i that denotes the voltage fluctuation of multilevel output. The larger capacitance has the fewer ripple voltage. The voltage fluctuation over a narrow scope has a smaller power losses and higher capacitor efficiency. The appropriated method of capacitance calculation is that the maximum voltage ripple is 10% of the maximum capacitor voltage [28].

Before obtaining the capacitance of C_i, two assumptions are given to simplify the derivations: 1) the output load is pure resistive load, and 2) the same duration is given in each level of staircase output. Therefore, the time points in Fig. 3 are

$$t_0 = 0, \quad t_1 = \frac{1}{20}t_s, \quad t_2 = \frac{1}{10}t_s, \quad t_3 = \frac{3}{20}t_s, \quad t_4 = \frac{1}{5}t_s$$
$$t_5 = \frac{3}{10}t_s, \quad t_6 = \frac{7}{20}t_s, \quad t_7 = \frac{2}{5}t_s, \quad t_8 = \frac{9}{20}t_s \tag{7}$$

where t_s is the period of the output voltage derived by

$$t_s = \frac{1}{f_s} \tag{8}$$

where f_s is the frequency of the output voltage. In the operational mode 1, as shown in Fig. 3(a), the longest discharging cycle of C_1 is between t_4 and t_5, and the longest discharging cycle of C_2 is between t_3 and t_6. In the operational mode 2, as shown in Fig. 3(b), the longest discharging cycle of C_1 is the same as the operational mode 1, while the longest discharging cycle of C_2 is between t_2 and t_7. Therefore, the maximum discharging amount of C_1 is Q_{c1} and is defined as

$$Q_{c1} = \int_{t_4}^{t_5} I_{\text{out}} \sin(2\pi f_s t - \Phi) dt \tag{9}$$

where I_{out} is the amplitude of the output current i_{out} and Φ is the phase difference between the output voltage v_o and current i_{out}. If 10% ripple voltage is considered, Q_{c1} should be less than 10% of the maximum charge of C_1, i.e.

$$C_1 \geq \frac{Q_{c1}}{0.1V_{\text{in}}}. \tag{10}$$

Furthermore, the maximum discharging amount of C_2 is Q_{c2} and is defined as

$$Q_{c2} = \int_{t_3}^{t_6} I_{\text{out}} \sin(2\pi f_s t - \Phi) dt, \quad \text{mode 1} \tag{11}$$

$$Q_{c2} = \int_{t_2}^{t_7} I_{\text{out}} \sin(2\pi f_s t - \Phi) dt, \quad \text{mode 2}. \tag{12}$$

Then

$$C_2 \geq \frac{Q_{c2}}{0.1V_{\text{in}}}. \tag{13}$$

It can be seen from the equations that the operational mode 2 needs larger C_2 than that in operational mode 1. When the load is resistive, the phase of load current is agreed with the load voltage. The maximum discharging amount of capacitor is obtained in resistive load, because the peak load current is the midpoint of integration period. In other words, if the capacitance of C_i is derived in pure resistive load, it also maintains the less voltage ripples in inductive load.

The peak current of the capacitor C_i is derived by

$$I_{ci} = \frac{V_{\text{in}} - V_{C_i} - V_{dF}}{r_c + r_{\text{on}} + r_d} \tag{14}$$

where V_{C_i} is the voltage on the capacitors C_i, V_{dF} is the forward voltage drop of diode, r_c is the equivalent series resistance (ESR) of the capacitors, r_{on} is the internal on-state resistance of the switching device, and r_d is the internal on-state resistance of the diode. Because of a small voltage difference of V_{in} and V_{C_i}, the peak current I_{ci} is fewer for the larger C_i. Thus, the larger capacitor is needed to cut down undesirable peak current and prolong the capacitor lifetime.

The analysis of switching loss is similar to the traditional cascaded H-bridge, while the capacitor losses consisting of ripple loss P_{rip} and conduction loss P_{cond} are newly introduced by the proposed inverter. When the capacitor C_i is connected from series to parallel, the ripple is derived by the difference between the input voltage V_{in} and the capacitor voltage V_{c_i}. The voltage ripple of C_i is

$$\Delta V_{\text{rip}} = \frac{1}{C_i} \int_{t_-}^{t_+} i_{C_i} dt \tag{15}$$

where i_{C_i} is the transient current of the capacitor C_i, and the discharging interval is denoted by t_- and t_+. For C_1 in operational mode 1, t_- and t_+ are t_4 and t_5, respectively. For C_2 in operational mode 1, t_- and t_+ are t_3 and t_6, respectively. Thus, the loss from voltage ripple is resulted by

$$P_{\text{rip}} = \sum_{i=1}^{k} C_i \Delta V_{\text{rip}}^2 f_s \tag{16}$$

where k is the number of switched capacitors (SCs), and f_s is the frequency of the output voltage. It can be found that the ripple loss is inversely proportional to the capacitor C_i. The conduction losses can be further calculated by

$$P_{\text{cond}} = 2f_s \sum_{i=1}^{k} \int_{t_-}^{t_+} r_c i_{ci}^2 dt. \tag{17}$$

The larger capacitor current leads to a large conduction loss. Lastly, the losses from SCs are denoted by

$$P_{sc} = P_{\text{rip}} + P_{\text{cond}}. \tag{18}$$

Both ripple loss and conduction loss are proportional to the frequency of the output voltage and number of capacitors. It is concluded that a larger capacitor can improve efficiency and

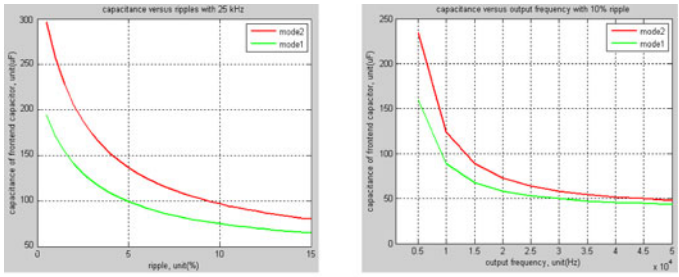


Fig. 8. Capacitance determination. (a) Curves of frontend capacitor versus voltage ripple with 25 kHz output frequency. (b) Curves of frontend capacitor versus output frequency with 10% voltage ripple.

prolong capacitor lifetime. However, the larger capacitor leads to the higher cost. Thus, a tradeoff of cost and efficiency need to be taken into account.

According to (10), (13), and (15), the relation curves of SCs (C_i) and ripple voltage are illustrated in Fig. 8(a) with the fixed 25 kHz output frequency, and relation curves of SC (C_i) and output frequency are illustrated in Fig. 8(b) with the fixed 10% ripple voltage.

It can be found from Fig. 8(a) that the less capacitance leads to larger ripple voltage. Operational mode 2 needs larger capacitance than mode 1 to keep the ripples low. The gradient of capacitor to ripple is larger in low-ripple zone, and the gradient of capacitor to ripple is lower in high-ripple zone. The gradient variation is caused by inversely proportional relation between capacitance with ripple voltage. It can be found from Fig. 8(b) that the less capacitance is required for higher frequency applications to maintain 10% ripple voltage. Thus, capacitor cost can be greatly saved for HF application compared with low-frequency counterpart.

IV. Further Enhancements

The number of voltage levels can be further increased via two approaches. One is to increase the level number generated by SC circuit; the other one is to increase level number generated by cascaded H-Bridge. Thirteen-level inverters, as shown in Fig. 9, explain these two methods.

A 3 × 2 structure, as shown in Fig. 9(a), is derived by the enhancement of SC circuit, which needs 6 diodes, 4 capacitors, 14 switches, and 2 dc inputs. 2 × 3 structure as shown in Fig. 9(b) is derived by the enhancement of H-Bridge circuit, which needs 3 diodes, 3 capacitors, 18 switches, and 3 dc inputs. It can be found that 3 × 2 structure requires more diodes and capacitors than 2 × 3 structure. However, the number of power switches in 3 × 2 structure is less than that in 2 × 3 structure. Because the traditional cascaded H-bridge needs 24 switches and 6 inputs to produce 13 voltage levels, the numbers of power switches and inputs are greatly decreased by proposed inverter. In order to accomplish the staircase output with $4n + 1$ voltage levels, the component counts are compared in Table II.

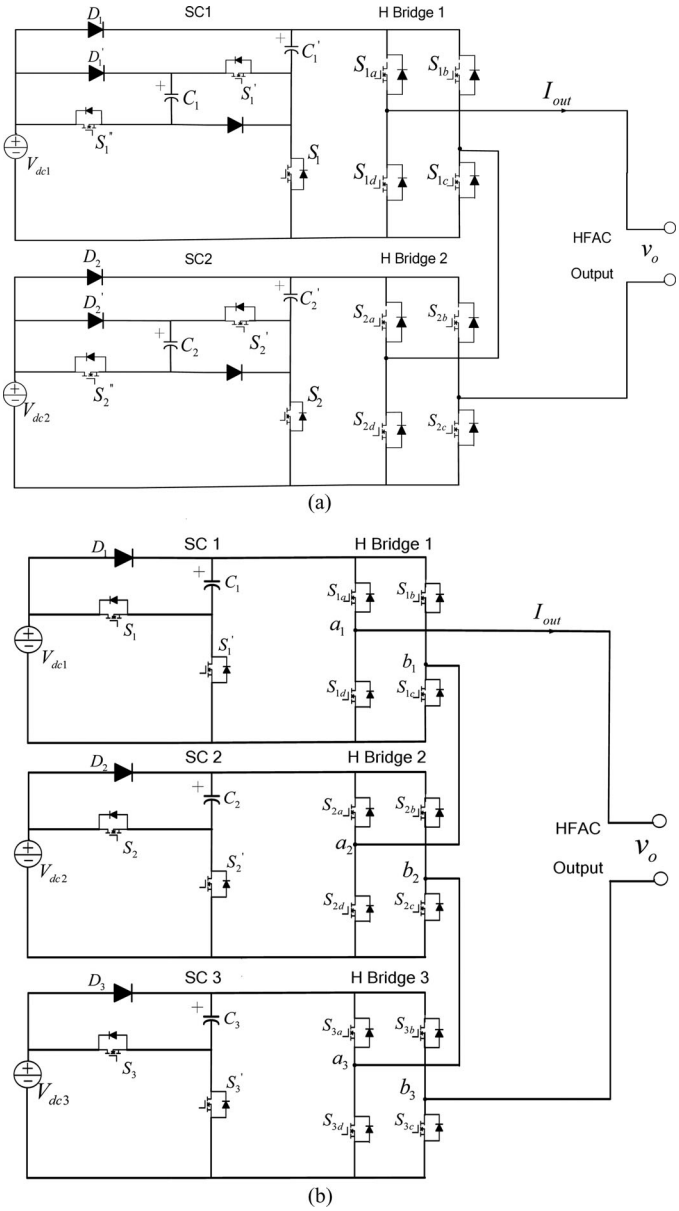


Fig. 9. Circuit topology of 13-level inverter. (a) 3 × 2 with two dc inputs. (b) 2 × 3 with three dc inputs.

TABLE II
Components Comparison of Proposed Inverter and Cascaded H-Bridge

Inverter type	Proposed inverter enhanced by SC n×2 topology	Proposed inverter enhanced by H-Bridge 2×n topology	Cascaded H-Bridge
Switching device	2n+8	6n	8n
Capacitor	2n-2	n	0
Diode	4n-6	n	0
DC bus	2	n	2n
Power losses	$(2n-2)loss_{cap}+(4n-6)loss_{diode}+(2n+8)loss_{switch}$	$nloss_{cap}+nloss_{diode}+6nloss_{switch}$	$8nloss_{switch}$

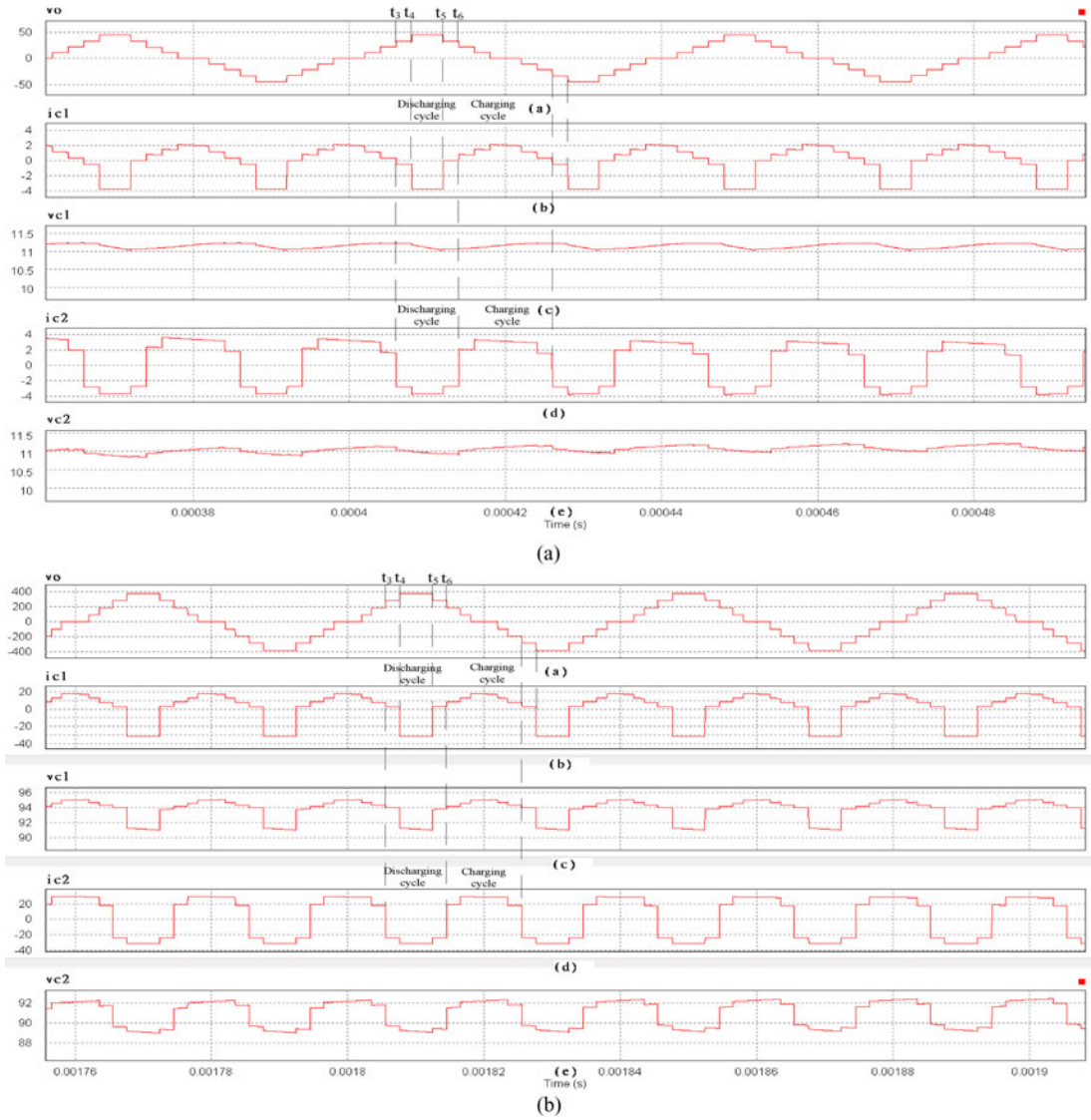


Fig. 10. Simulation waveforms of nine-level SC-based cascaded inverter, output frequency f_s = 25 kHz ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$, mode 1). (a) Low power at 50 W. (b) High power at 4 kW.

An $n \times 2$ topology needs $2n - 2$ capacitors, $2n + 8$ switches, and 2 dc inputs; $2 \times n$ topology needs n capacitors, $6n$ switches, and n dc inputs. The traditional cascaded H-Bridge needs $8n$ switches and $2n$ dc inputs. With the same number of voltage levels, the proposed inverter needs less switching devices and inputs than the traditional cascaded H-Bridge. Considering the power losses, the traditional cascaded H-bridge has the higher switching losses caused by more switch devices. However, the proposed inverter newly introduces the capacitor loss that has already been examined in last section. Moreover, a flexible circuit structure becomes possible. It is feasible for the proposed multilevel inverter to select suitable enhancement that can accommodate the requirements from different applications. For example, $2 \times n$ topology can be used for the power application sourced by multiple solar panels or batteries, and $n \times 2$ topology can be used for the power application sourced by dual power sources.

V. Performance Evaluation

A. Simulation Evaluation

The simulation based on PSIM is performed for the proposed inverter. The waveforms of output voltage v_o, capacitor currents (i_{C1}, i_{C2}) and capacitor voltages (v_{C1}, v_{C2}) are shown in Fig. 10. The following parameters are used for low power simulation. The input voltage is $V_{\text{in}} = 12$ V, the module 1 capacitor is $C_1 = 100$ μF with 80 mΩ ESR, the module 2 capacitor is $C_2 = 220$ μF with 50 mΩ ESR, the diodes D_1 and D_2 have 0.6 V forward voltage drop and 50 mΩ internal on-state resistance, and the load resistance is $R_o = 12$ Ω. The following parameters are used for high-power simulation. The input voltage is $V_{\text{in}} = 100$ V, the module 1 capacitor is $C_1 = 300$ μF with 30 mΩ ESR, the module 2 capacitor is $C_2 = 560$ μF with 20 mΩ ESR, and the load resistance is $R_o = 12$ Ω. The output frequency f_s is 25 kHz. The waveforms of low power and high power are

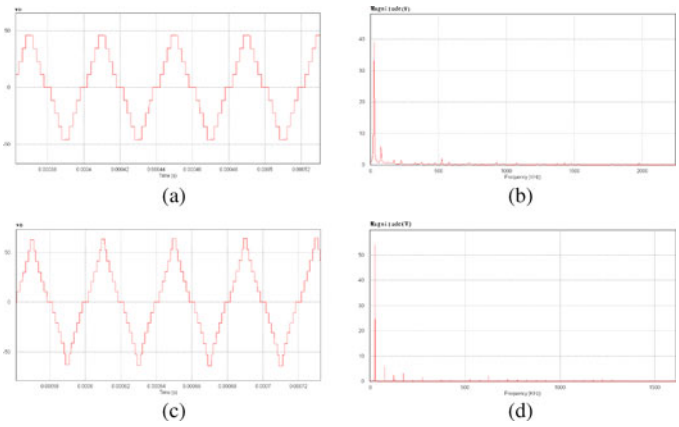


Fig. 11. Simulation waveforms of 9-level and 13-level inverter, output frequency $f_s = 25$ kHz. (a) Output voltage of nine-level inverter ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$). (b) Spectrum of nine-level output. (c) Output voltage of 13-level inverter (same duration of each voltage level). (d) Spectrum of 13-level output.

demonstrated in Fig. 10(a) and (b), respectively. It can be seen that the proposed inverter can work at higher power. C_1 and C_2 can be converted to resonant switched-capacitor topology easily [29], [30] and hence the less power loss can be achieved in the frontend SC stage.

The simulation waveforms are accorded with theoretical analysis. C_1 is discharged at the interval of t_4 to t_5, and C_2 is discharged at the interval of t_3 to t_6. Both capacitors are charged and discharged once every half cycle. Because of the internal resistance of diodes D_1 and D_2, the charging current can be divided into several subintervals that are in accordance with operational analysis in Fig. 4. Considering the charging cycle and *RC* time constant, the peak current of charging period and voltage drop of discharging period are rational at the given conditions. Theoretically, low power can obtain amplitude of $\pm 4 \times 12$ V, and high power can obtain amplitude of $\pm 4 \times 100$ V. However, an amplitude difference emerges between theoretical results and simulation waveforms. In low power simulation, the voltage of the capacitors C_1 varies between 11 and 11.3 V, while the voltage of the capacitors C_2 varies between 10.8 and 11.1 V. In high power simulation, the voltage of the capacitors C_1 varies between 91 and 95 V, while the voltage of the capacitors C_2 varies between 89 and 91 V. Thus, the amplitude of simulation waveform is less than the theoretical amplitude caused by forward voltage drop and inner resistance.

The output voltage and voltage spectrum are compared in Fig. 11, including 9- and 13-level inverter. Fig. 11(a) is output waveform of nine-level inverter at condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, and $x_2 = \pi/4$. The voltage step in staircase output has a slightly drop at $t = 0.00465$–0.00475 due to the discharging cycle of SC. Fig. 11(c) is output waveform of 13-level inverter with the same duration of each voltage level. A thirteen-level inverter adopts 3×2 structure, and the following circuit parameters are used. The input voltage is $V_{\text{in}} = 12$ V, the module 1 capacitors are $C_1 = 100\ \mu$F $C_1' = 120\ \mu$F with 80 mΩ ESR, the module 2 capacitor are $C_2 = 220\ \mu$F $C_2' = 250\ \mu$F with 50 mΩ ESR, and the load resistance is $R_o = 12\ \Omega$. It can be found from Fig. 11(c) that the voltage drop is indistinctive in each step of staircase output because the discharging periods of SCs become shorter for 13-level inverter.

TABLE III
HARMONICS OF THE PROPOSED 9-LEVEL AND 13-LEVEL INVERTER

Harmonic	9-level	13-level
Fundamental 1	38.8V	55.1V
3	6.8V	7.2V
5	2.6V	2.1V
7	1V	2V
9	1V	0.5V
THD(%)	19.1	14.1

The output spectrums of 9-level and 13-level inverter are illustrated in Fig. 11(b) and (d), respectively. The fundamental frequency is 25 kHz that is the same as output frequency. It can be observed that the fundamental harmonic is significantly higher than the other harmonics. The magnitude of fundamental component is below 40 V for nine-level inverter, while the magnitude of fundamental component is 55 V for a 13-level inverter. The dominating harmonics are compared in Table III. The calculated THD is 19.1% for 9-level inverter and 14.1% for 13-level inverter. A 13-level inverter has fewer high order harmonics than nine-level inverter. It can be estimated that the harmonics can be further cut down along with the increasing number of voltage levels. Thus, the proposed inverter produces near sinusoidal staircase output, and two methods can make it more sinusoidal. One is to optimize the duration of voltage levels; the other one is to increase the number of voltage levels.

B. Experimental Evaluation

An experimental prototype was implemented with output frequency of 25 kHz and output power of 50 W. The schematic of modulation circuit is shown in Fig. 12 that is made up of DFF, RSFF, NOT, and XOR. LM393 is a dual comparator operated at single voltage mode. The LOCMOS logic components consisting of HEF4013 (dual D flip-flop), HEF4070 (Quad 2-input XOR), HEF4081 (Quad 2-input AND gate), and HEF4069 (Hex Inverters) accomplish the symmetrical PSM. 5 V output in CMOS logic is magnified by boot-strap IC IR2113 to drive power switches. The schematic of power circuit is same as shown in Fig. 1. The switching devices are IRF540 MOSFETs with about 50 mΩ on-state resistances. Capacitor C_1 is 100 μF electrolytic capacitor with ESR 80 mΩ, while C_2 is 220 μF electrolytic capacitor with ESR 50 mΩ. V_{in} is 12 V supplied by dc power supply KIKUSUI PAS40-9. The switching frequency of H-bridge backend is 25 kHz, while the switching frequency of SC frontend is 50 kHz. R_o is 12 Ω resistive load.

Fig. 13 shows the observed waveforms of gate drivers (g_{s1}, gs_{1a}), input currents $(I_{\text{in1}}, I_{\text{in2}})$, and output voltage (v_o). The switching frequency of S_1, S_1', S_2, and S_2' is twice the output frequency, and the switching frequency of $S_{1a} - S_{1d}$ and $S_{2a} - S_{2d}$ is the same as the output frequency. Thus, the switching frequency is so much less than that in multicarrier modulation. I_{in2} is greater than I_{in1}, so V_{dc2} provides more

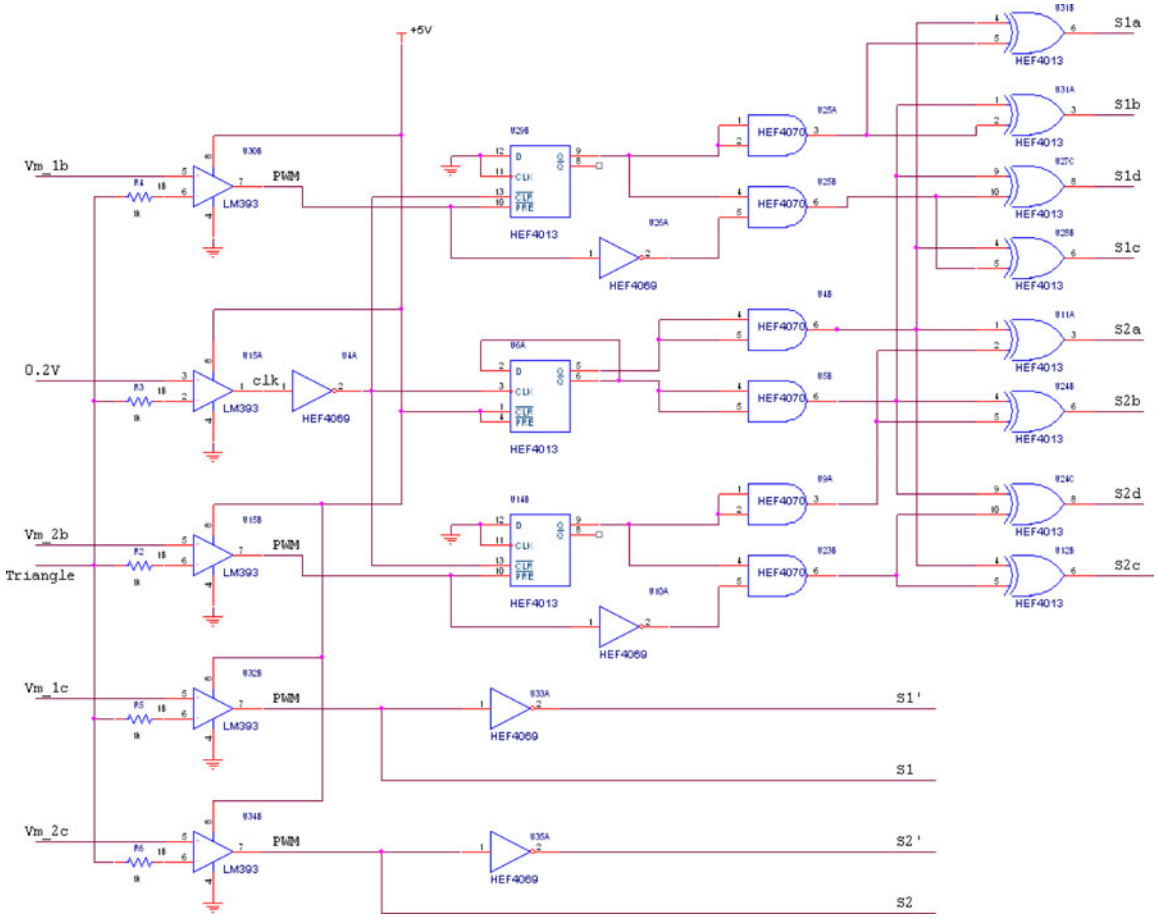


Fig. 12. Schematic of modulation circuit.

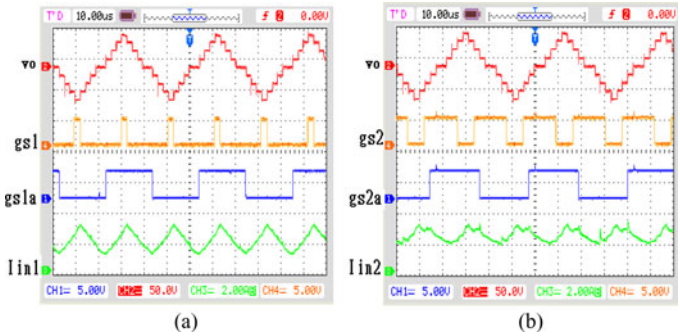


Fig. 13. Observed waveforms of output voltage, gate drivers, input currents with 25 kHz frequency and 12 Ω load ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$). (a) Upper trace: output voltage v_o; second trace: S_1 gate driver g_{s1}; third trace: S_{1a} gate driver of g_{s1a}; lower trace: input current $I_{\text{in}1}$. (b) Upper trace: output voltage v_o; second trace: S_2 gate driver g_{s2}; third trace: S_{2a} gate driver g_{s2a}; lower trace: input current $I_{\text{in}2}$.

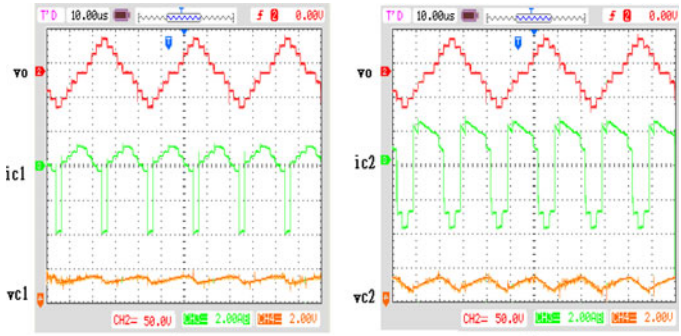
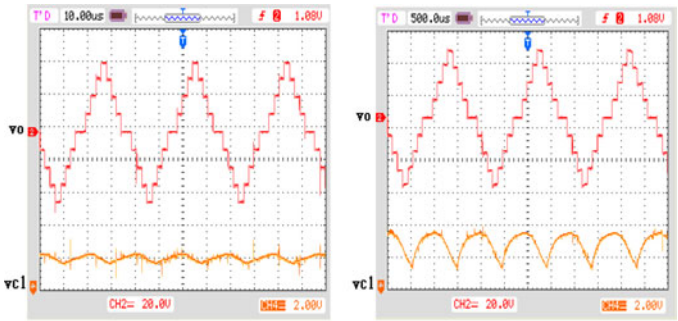


Fig. 14. Observed waveforms of output voltage, capacitor currents and capacitor voltages with 25 kHz output frequency, and 12 Ω load ($k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$). (a) Upper trace: output voltage v_o; middle trace: capacitor current i_{c1}; lower trace: capacitor voltage v_{c1}. (b) Upper trace: output voltage v_o; middle trace: capacitor current i_{c2}; lower trace: capacitor voltage v_{c2}.

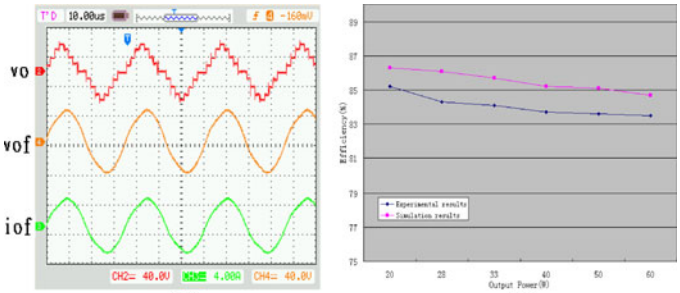
energy than V_{dc1}. There is an energy unbalance in each cell with cascaded connection, and the further study is required for power balance. THD of output voltage is 19.7% for nine-level inverter, which is close to simulation results and theoretical analysis.

Fig. 14 shows the observed waveforms of output voltage (v_o), capacitor currents (i_{c1}, i_{c2}), and capacitor voltages (v_{c1}, v_{c2}). The observed amplitude of output voltage is lower than the theoretical amplitude 48 V caused by the voltage drop from the internal resistance of MOSFETs, diode, and capacitor. The charging cycle is divided into several subintervals, and capacitor C_1 has a shorter discharging cycle than capacitor C_2. The capacitor voltages v_{c1} and v_{c2} alternatively increase and drop along with charging and discharging operations, respectively. v_{c1} has the lower ripple voltage than v_{c2} due to the shorter



(a) (b)

Fig. 15. Observed output and capacitor voltage at condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$, and 12 Ω load. (a) Output waveforms of 25 kHz frequency. Upper trace: output voltage v_o; lower trace: capacitor voltage v_{c1}. (b) Output waveforms of 500 Hz frequency. Upper trace: output voltage v_o; lower trace: capacitor voltage v_{c1}.



(a) (b)

Fig. 16. Output waveforms after *LC* filter and conversion efficiency. (a) Upper trace: staircase output v_o; middle trace: output voltage after *LC* filter $v_{\rm of}$; lower trace: output current after *LC* filter $i_{\rm of}$. (b) Conversion efficiency comparisons of nine-level inverter with 25 kHz output under the condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$.

discharging period. The experimental results are in accord with the simulation waveforms as shown in Fig. 10.

Fig. 15 shows the observed waveforms at the different output frequencies with the operational condition of $k_1 = k_2 = 0.5$, $x_1 = \pi/8$, $x_2 = \pi/4$. The same circuit parameters are adopted for comparisons of 25 kHz and 500 Hz. The output and capacitor voltage are demonstrated in Fig. 15(a) with the output frequency of 25 kHz; the output and capacitor voltage are demonstrated in Fig. 15(b) with the output frequency of 500 Hz. It can be found that the voltage drop is indistinct in each step of 25 kHz staircase output caused by a shorter discharging cycle. However, a larger voltage drop occurs in each step of 500 Hz staircase output due to a longer discharging cycle. Likewise, the larger ripple can be found in capacitor voltage v_{c1} with output frequency of 500 Hz.

A small *LC* filter is added in front of resistive load to improve the output harmonics. The filter inductor and capacitor are 50 μH and 0.5 μF, respectively. Output voltage and current after filter are $v_{\rm of}$ and $i_{\rm of}$, both of which are demonstrated in Fig. 16(a). It can be found that the *LC* filter smoothes the staircase output and more sinusoidal output is obtained for power distribution.

The efficiency curves of the simulation and experiment are illustrated in Fig. 16(b). Both simulation and experiment adopt the same circuit parameters with the output frequency of 25 kHz. There are some small differences existed between the results of simulation and experiment due to the discrepancy between the simulation model and the experimental prototype. However, the curvature varied with the output current is almost similar. The main power losses contain switching losses, conduction losses of the switches, conduction losses of capacitors, and ripple losses of capacitors. It can be found that the proposed inverter can achieve more than 83% conversion efficiency over a wide range of output current. Meanwhile, total efficiency slightly falls off along with the increase in the output power. The root cause is the increase of conduction losses due to on-resistance of the power MOSFET.

With the same circuit parameters, the smooth output is seen in high-frequency scenario. Meanwhile, the capacitor cost of high-frequency scenario can be significantly saved compared with low frequency counterpart. Thus, the proposed modulation and topology are more suitable for high-frequency applications. Furthermore, the charging and discharging frequencies of SCs are twice the output frequency, which is significantly less than the charging and discharging frequencies in multicarrier pulsewidth modulation [18]. Thus, the capacitor lifetime is prolonged by the reduced times of charging and discharging. Meanwhile, the system reliability is increased due to the same circuit cell and modulation strategy. It is concluded from simulation and experiment that the proposed multilevel inverter and symmetrical modulation are an effective approach to serve as high-frequency power source with higher conversion efficiency.

VI. Conclusion

In this paper, a novel SC-based cascaded multilevel inverter was proposed. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method.

Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases twice in half cycle of 9-level circuit, and the number of voltage levels increases three times in half cycle of 13-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be accomplished by pulsewidth regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This paper mainly analyzes nine-level and 13-level inverters. The method of analysis and design is also applicable to other members of the proposed inverter. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultracapacitors, and fuel cells.

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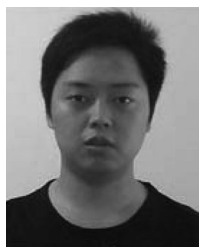

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